REMARKS

I. Introduction

Claims 9-16 are pending in the present application. In view of the following remarks, it is respectfully submitted that claims 9-16 are allowable, and reconsideration is respectfully requested.

Applicants thank the Examiner for the acknowledgement of the claim for foreign priority, as well as the indication that certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

II. Rejection of Claims 9-11 and 13-16 under 35 U.S.C. §103(a)

Claims 9-11 and 13-16 were rejected under 35 U.S.C. §103(a) as being unpatentable over US 20010044862 ("Mergard"). Applicants respectfully submit that claims 9-11 and 13-16 are not rendered obvious by Mergard, for at least the reasons set forth below.

In rejecting a claim under 35 U.S.C. § 103(a), the Office bears the initial burden of presenting a prima facie case of obviousness. In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). To establish prima facie obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine the reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). The prior art must suggest combining the features in the manner contemplated by the claim. See Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 934 (Fed. Cir. 1990), cert. denied, 111 S. Ct. 296; In re Bond, 910 F.2d 831, 834 (Fed. Cir. 1990). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim features. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). To the extent that the Examiner may be relying on the doctrine of inherent disclosure for the anticipation rejection, the Examiner must provide a "basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristics necessarily flow from the teachings of the applied art." (See M.P.E.P. § 2112; emphasis in original; see also Ex parte Levy, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990)).

Independent claim 9 recites, in relevant part, "transmitting in parallel at least two signals unidirectionally on at least two signal paths, . . . the at least two signals being routed in parallel on the at least two signal paths into the at least two register cells of the first shift register; transmitting data corresponding to the at least two signals serially from the first shift register to the second shift register by **automatically clocking the register cells** of the first shift register and the second shift register from **a time base directly connected to the register cells**, . . . wherein each transmitting is performed **without loading a CPU**." Independent claim 15 recites substantially similar features as the above-recited features of claim 9. In support of the rejection, the Examiner makes the following contentions: a) "Mergard discloses a method for serially transmitting data between a first station (406; Fig. 4) and a second station (418; Fig. 4)"; b) "In Figure 1 the processor is element 100 and Figure 2 discloses the bus controller and additionally includes a serial bus controller"; and c) "Mergard thus appears to not load the processor 100." Applicants respectfully submit that even if the assertions a) and b) noted above are true, the conclusion c) is simply unsupported, as explained in detail below.

As clearly shown in Fig. 1, the embedded controller C has a processor 100 coupled to a timer 102 by an internal bus 110 (par. [0015]), and Fig. 2 clearly shows the details of a converter 200 (par. [0019]). In addition, as explained in connection with Fig. 3, when a first embedded controller 300 wishes to transfer information to a second embedded controller 306 or 310, the first "**embedded controller 300 transfers the parallel data, address, and control information to the converter 202A**" assigned to the first embedded controller 300, and the converter 202A performs the parallel-to-serial conversion and transfers the information to the converter assigned to the second embedded controller 306 or 310. (Par. [0026]). Furthermore, as explained in connection with Fig. 2, "[t]he configuration register 202 [of converter 200] receives **data from a system data bus of the embedded controller C**," as well as receiving "**addresses from a system address bus of the embedded controller C**," and "**[b]ased upon an address on the system address bus**, the configuration register 202 can be set-up to enable or disable the system control, address, and data buses coupled to the parallel bus transceiver/multiplexer unit 208." (Par. [0020]). Based on the above description, it is quite clear that the processor 100 of the embedded controller is involved in the data transmission via the converter, i.e., the CPU is clearly loaded by the data transmission.

For at least the foregoing reasons, claims 9 and 15, as well as their dependent claims 10-11, 13-14 and 16, are allowable over Mergard. Withdrawal of the obviousness rejection is requested.

III. Rejection of Claims 9-16 under 35 U.S.C. § 103(a)

Claims 9-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Shimada (JP 11-178349). Applicants respectfully submit that claims 9-16 are not rendered obvious by Shimada, for at least the reasons set forth below.

In rejecting a claim under 35 U.S.C. § 103(a), the Office bears the initial burden of presenting a prima facie case of obviousness. In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). To establish prima facie obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine the reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). The prior art must suggest combining the features in the manner contemplated by the claim. See Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 934 (Fed. Cir. 1990), cert. denied, 111 S. Ct. 296; In re Bond, 910 F.2d 831, 834 (Fed. Cir. 1990). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim features. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). To the extent that the Examiner may be relying on the doctrine of inherent disclosure for the anticipation rejection, the Examiner must provide a "basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristics necessarily flow from the teachings of the applied art." (See M.P.E.P. § 2112; emphasis in original; see also Ex parte Levy, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990)).

Independent claim 9 recites, in relevant part, "transmitting in parallel at least two signals unidirectionally on at least two signal paths, . . . the at least two signals being routed in parallel on the at least two signal paths into the at least two register cells of the first shift register; transmitting data corresponding to the at least two signals serially from the first shift register to the second shift register by **automatically clocking the register cells** of the first shift register and the second shift register from **a time base directly connected to the**

register cells, . . . wherein each transmitting is performed **without loading a CPU**." Independent claim 15 recites substantially similar features as the above-recited features of claim 9. In support of the rejection, the Examiner contends that Yamada discloses a clock circuit 11, a serial-to-parallel circuit 12 (this is incorrect: element 12 is a parallel-to-serial circuit), and a parallel-to-serial circuit 14 (this is incorrect: element 14 is a serial-to-parallel circuit). In addition, the Examiner contends that "Yamada does not discuss the clock rate in the abstract but it would have been obvious to select a clock of sufficient speed such that bits would not be missed." Applicants respectfully submit that the actual teachings of Yamada are woefully inadequate to support an obviousness rejection, as explained in detail below.

First, there is absolutely no indication in the English Abstract of Yamada that element 11 is indeed a clock circuit. Second, even if one assumes for the sake of argument that element 11 is indeed a clock circuit, there is absolutely no suggestion that the element 11 in anyway automatically clocks the parallel-to-serial circuit 12 to serially transmit signals. Third, even if one assumes for the sake of argument that the parallel-to-serial circuit 12 is somehow equivalent to the claimed "first shift register" of the first station, there is absolutely no suggestion of automatically clocking the first shift register of a first station to serially transmit data to a second shift register of a second station, since Yamada clearly indicates that both conversion circuits 12 and 14 are part of the same pulse-width-modulation control device. Fourth, there is absolutely no affirmative indication or suggestion that "each transmitting is performed **without loading a CPU**."

For at least the foregoing reasons, claims 9 and 15, as well as their dependent claims 10-14 and 16, are allowable over Yamada. Withdrawal of the obviousness rejection is requested.

IV. Rejection of Claims 9-11 and 13-16 under 35 U.S.C. § 103(a)

Claims 9-11 and 13-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,475,831 ("Yoshida"). Applicants respectfully submit that claims 9-11 and 13-16 are not rendered obvious by Yoshida, for at least the reasons set forth below.

In rejecting a claim under 35 U.S.C. § 103(a), the Office bears the initial burden of presenting a prima facie case of obviousness. In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). To establish prima facie obviousness, three criteria

must be satisfied. First, there must be some suggestion or motivation to modify or combine the reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). The prior art must suggest combining the features in the manner contemplated by the claim. See Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 934 (Fed. Cir. 1990), cert. denied, 111 S. Ct. 296; In re Bond, 910 F.2d 831, 834 (Fed. Cir. 1990). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim features. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). To the extent that the Examiner may be relying on the doctrine of inherent disclosure for the anticipation rejection, the Examiner must provide a "basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristics necessarily flow from the teachings of the applied art." (See M.P.E.P. § 2112; emphasis in original; see also Ex parte Levy, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990)).

Independent claim 9 recites, in relevant part, "transmitting in parallel at least two signals unidirectionally on at least two signal paths, . . . the at least two signals being routed in parallel on the at least two signal paths into the at least two register cells of the first shift register; transmitting data corresponding to the at least two signals serially from the first shift register to the second shift register by **automatically clocking the register cells** of the first shift register and the second shift register from **a time base directly connected to the register cells**, . . . wherein **each transmitting is performed without loading a CPU**." Independent claim 15 recites substantially similar features as the above-recited features of claim 9. In support of the rejection, the Examiner contends that "Yoshida discloses a serial transmission system that includes a shift register for the serialization/deserialization function and is driven by the clocking circuitry," which shift register is "fed from the buffer which provides isolation . . . such that the CPU does not need to directly control the serialization." The Examiner further contends that since "Yoshida discloses that this arrangement reduces the load on the CPU (col. 4, line 1), . . . it would have been obvious that the serializer transmits without loading the CPU." Applicants respectfully submit that the actual disclosure of Yoshida fails to support the Examiner's obviousness conclusion, as explained in detail below.

With respect to the Examiner's reliance on the statement of Yoshida that "the load of CPU is decreased," this statement does not mean that the data transmission does not load the CPU; instead, the statement merely refers to the fact that the CPU 32 does not have to access the buffer 34 each time a single byte is written into the buffer 34 (col. 3, l. 50-53), which remedies the disadvantage of the prior art discussed in Yoshida (see, e.g., col. 2, l. 46-49: "there are disadvantages in that the load of the CPU 12 becomes large, because the CPU 12 has to access the buffer 14 for each on byte transfer in response to the write request signal 300"). What Yoshida discloses is that two parallel data P_0 (each having two bytes) are "transferred for the CPU 32 to the buffer 34 by the write signals WR1 and WR2," and for each parallel data of two bytes, "read and load" signal (RD1/RD2) transfers the parallel data of two bytes into the shift register 36, which in turn generates serial data. However, it is absolutely clear that the data transmission via the buffer 34 and shift register 36 clearly involves (i.e., loads) CPU 32, since the data transmission clearly depends on the write signals (e.g., WR1 and WR2) written by the CPU 32. In view of the above, Applicants submit that Yoshida clearly fails to teach or suggest "transmitting in parallel at least two signals unidirectionally on at least two signal paths, . . . the at least two signals being routed in parallel on the at least two signal paths into the at least two register cells of the first shift register; **transmitting data** corresponding to the at least two signals serially from the first shift register to the second shift register by **automatically clocking the register cells** of the first shift register and the second shift register from **a time base directly connected to the register cells**, . . . wherein **each transmitting is performed without loading a CPU**."

For at least the foregoing reasons, Applicants submit that claims 9 and 15, as well as their dependent claims 10, 11, 13, 14 and 16, are allowable over Yoshida.

CONCLUSION

It is therefore respectfully submitted that the pending claims 9-16 are allowable. All issues raised by the Examiner have been addressed, and an early and favorable action on the merits is solicited.

Respectfully submitted,

KENYON & KENYON LLP

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By: JONG LEE for Gerard Messina

Gerard A. Messina
Registration Number 35,952
One Broadway
New York, New York 10004
(212) 425-7200
CUSTOMER NUMBER 26646